

I Claim:

- 1 1. An apparatus for effecting a controlled startup of a processor device; the apparatus
2 comprising:
3 (a) a first signal-treating circuit coupled with a voltage supply locus; said first
4 signal-treating circuit receiving a voltage supply signal and producing a first
5 treated signal representing said voltage supply signal;
6 (b) a second signal-treating circuit coupled with said voltage supply locus; said
7 second signal-treating circuit receiving said voltage supply signal and producing a
8 second treated signal representing said voltage supply signal; and
9 (c) a comparing unit; said comparing unit having a first input locus coupled with
10 said first signal-treating circuit and receiving said first treated signal; said
11 comparing unit having a second input locus coupled with said second signal-
12 treating circuit and receiving said second treated signal; said comparing unit
13 generating an output signal at an output locus when said first treated signal has a
14 predetermined relationship with said second treated signal; said output locus being
15 coupled with said processor device; said output signal effecting said controlled
16 startup.
- 1 2. An apparatus for effecting a controlled startup of a processor device as recited in
2 Claim 1 wherein said processor device includes a reset control pin; signals applied to
3 said reset control pin controlling a reset operation of said processor device; said
4 output locus being coupled with said reset control pin.
- 1 3. An apparatus for effecting a controlled startup of a processor device as recited in
2 Claim 1 wherein said first treated signal is a time-delayed representation of said
3 voltage supply signal and wherein said second treated signal is a non-delayed
4 representation of said voltage supply signal.
- 1 4. An apparatus for effecting a controlled startup of a processor device as recited in
2 Claim 2 wherein said first treated signal is a time-delayed representation of said

- 3 voltage supply signal and wherein said second treated signal is a non-delayed
4 representation of said voltage supply signal.
- 1 5. An apparatus for effecting a controlled startup of a processor device as recited in
2 Claim 1 wherein said comparing unit is a comparator.
- 1 6. An apparatus for effecting a controlled startup of a processor device as recited in
2 Claim 5 wherein said processor device includes a reset control pin; signals applied to
3 said reset control pin controlling a reset operation of said processor device; said
4 output locus being coupled with said reset control pin.
- 1 7. An apparatus for effecting a controlled startup of a processor device as recited in
2 Claim 5 wherein said first treated signal is a time-delayed representation of said
3 voltage supply signal and wherein said second treated signal is a non-delayed
4 representation of said voltage supply signal.
- 1 8. An apparatus for effecting a controlled startup of a processor device as recited in
2 Claim 6 wherein said first treated signal is a time-delayed representation of said
3 voltage supply signal and wherein said second treated signal is a non-delayed
4 representation of said voltage supply signal.
- 1 9. An apparatus for controlling operation of a processor device during startup of said
2 processor device; the apparatus comprising:
3 (a) a signal treating circuit receiving a voltage supply signal at a voltage supply
4 locus; said signal treating circuit using said voltage supply signal for generating a
5 first treated signal and a second treated signal; and
6 (b) an output circuit coupled with said signal treating circuit; said output circuit
7 receiving said first treated signal and said second treated signal and generating a
8 control signal at an output locus based upon a relationship between said first

9 treated signal and said second treated signal; said output locus being coupled with
10 said processor device; said control signal effecting said controlling.

1 10. An apparatus for controlling operation of a processor device during startup of said
2 processor device as recited in Claim 9 wherein said processor device includes a reset
3 control pin; signals applied to said reset control pin controlling a reset operation of
4 said processor device; said output locus being coupled with said reset control pin.

1 11. An apparatus for controlling operation of a processor device during startup of said
2 processor device as recited in Claim 9 wherein said first treated signal is a time-
3 delayed representation of said voltage supply signal and wherein said second treated
4 signal is a non-delayed representation of said voltage supply signal.

1 12. An apparatus for controlling operation of a processor device during startup of said
2 processor device as recited in Claim 10 wherein said first treated signal is a time-
3 delayed representation of said voltage supply signal and wherein said second treated
4 signal is a non-delayed representation of said voltage supply signal.

1 13. An apparatus for controlling operation of a processor device during startup of said
2 processor device as recited in Claim 9 wherein said output circuit comprises a
3 comparator.

1 14. An apparatus for controlling operation of a processor device during startup of said
2 processor device as recited in Claim 13 wherein said processor device includes a reset
3 control pin; signals applied to said reset control pin controlling a reset operation of
4 said processor device; said output locus being coupled with said reset control pin.

1 15. An apparatus for controlling operation of a processor device during startup of said
2 processor device as recited in Claim 13 wherein said first treated signal is a time-

3 delayed representation of said voltage supply signal and wherein said second treated
4 signal is a non-delayed representation of said voltage supply signal.

1 16. An apparatus for controlling operation of a processor device during startup of said
2 processor device as recited in Claim 14 wherein said first treated signal is a time-
3 delayed representation of said voltage supply signal and wherein said second treated
4 signal is a non-delayed representation of said voltage supply signal.

1 17. A method for controlling operation of a processor device during startup of said
2 processor device; the method comprising the steps of:
3 (a) in no particular order:
4 (1) providing a signal treating circuit; and
5 (2) providing an output circuit coupled with said signal treating circuit;
6 (b) operating said signal treating circuit to receive a voltage supply signal at at
7 least one voltage supply locus;
8 (c) operating said signal treating circuit to use said voltage supply signal for
9 generating a first treated signal and a second treated signal;
10 (d) operating said output circuit to receive said first treated signal and said second
11 treated signal;
12 (e) operating said output circuit to generate a control signal at an output locus;
13 said control signal being based upon a relationship between said first treated
14 signal and said second treated signal; and
15 (f) providing said control signal to said processor device for effecting said
16 controlling.

1 18. A method for controlling operation of a processor device during startup of said
2 processor device as recited in Claim 17 wherein said processor device includes a reset
3 control pin; signals applied to said reset control pin controlling a reset operation of
4 said processor device; said output locus being coupled with said reset control pin.

1 19. A method for controlling operation of a processor device during startup of said
2 processor device as recited in Claim 18 wherein said output circuit comprises a
3 comparator.

1 20. A method for controlling operation of a processor device during startup of said
2 processor device as recited in Claim 19 wherein said first treated signal is a time-
3 delayed representation of said voltage supply signal and wherein said second treated
4 signal is a non-delayed representation of said voltage supply signal.